	Application No.	Applicant(s)
AL 41	10/705,895	OGIHARA ET AL.
Notice of Allowability	Examiner	Art Unit
	Hai C. Pham	2861
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to <u>Amendment filed 12/14/06</u> .		
2. The allowed claim(s) is/are <u>1-58</u> .		
3.		
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal F 6. ☐ Interview Summary Paper No./Mail Da 7. ☐ Examiner's Amenda 8. ☑ Examiner's Stateme 9. ☐ Other	(PTO-413), te

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REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: claims 1 and 1. 28 are allowed at least for the reason that the prior art of record does not teach or reasonably suggest the specific structure of the combined semiconductor apparatus, which comprises a substrate, a first thin semiconductor film comprised of a first material and being disposed on and bonded to a surface of the substrate, the first thin semiconductor film including at least one semiconductor device, a second thin semiconductor film comprised of a second material that is different than the first material and being disposed on and bonded to the same surface side of the substrate as the first thin semiconductor film, the second thin semiconductor film including an integrated circuit and a first terminal, and a first individual interconnecting line formed as a thin film extending from an upper side of the first thin semiconductor film over said surface of the substrate to an upper side of the second thin semiconductor film, electrically connecting the semiconductor device in the first thin semiconductor film to the first terminal in the second thin semiconductor film, with claim 28 further including the first and second thin semiconductor films being less than or equal to ten micrometers thick, as set forth in the claimed combination.

Claim 58 is allowed at least for the reason that the prior art of record does not teach or reasonably suggest the specific structure of the combined semiconductor apparatus, which comprises a substrate, a first thin semiconductor film comprised of a first material and being disposed on and bonded to a surface of the substrate, the first thin semiconductor film including at least one semiconductor device, a second thin

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semiconductor film comprised of a second material that is different than the first material and being disposed on and bonded to the same surface side of the substrate as the first thin semiconductor film, the second thin semiconductor film including an integrated circuit and a first terminal, and a first individual interconnecting line formed as a thin film extending from the first thin semiconductor film over said surface of the substrate to the second thin semiconductor film, electrically connecting the semiconductor device in the first thin semiconductor film to the first terminal in the second thin semiconductor film, a circuit pattern formed on the substrate, the circuit pattern comprising at least one of an interconnecting line, a resistor, and a capacitor, and a second individual interconnecting line formed as a thin film, wherein said second thin semiconductor film has a second terminal, the circuit pattern formed on the substrate has a third terminal, and the second individual interconnecting line extends from the second thin semiconductor film to the circuit pattern on the substrate, electrically interconnecting the second terminal with the third terminal, as set forth in the claimed combination.

Claims 2-27 and 29-57 are allowed because they are directly or indirectly dependent from claims 1 and 28 above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Luu can be reached on (571) 272-7663. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HAI PHAM
PRIMARY EXAMINER

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March 13, 2007